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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/796,023	03/10/2004	Kiyoo Itoh	520.40847CC2	2141
20457	7590	06/29/2004	EXAMINER	
ANTONELLI, TERRY, STOUT & KRAUS, LLP 1300 NORTH SEVENTEENTH STREET SUITE 1800 ARLINGTON, VA 22209-9889				AUDUONG, GENE NGHIA
ART UNIT		PAPER NUMBER		
				2818

DATE MAILED: 06/29/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

<b>Office Action Summary</b>	Application No.	Applicant(s)	
	10/796,023	ITOH ET AL. <i>EA</i>	
	Examiner Gene N Aduong	Art Unit 2818	

-- The MAILING DATE of this communication appears on the cover sheet with the corresponding address --  
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

#### Status

- 1) Responsive to communication(s) filed on \_\_\_\_.
- 2a) This action is FINAL.                            2b) This action is non-final.
- 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

#### Disposition of Claims

- 4) Claim(s) 1-20 is/are pending in the application.
- 4a) Of the above claim(s) \_\_\_\_ is/are withdrawn from consideration.
- 5) Claim(s) \_\_\_\_ is/are allowed.
- 6) Claim(s) 1-20 is/are rejected.
- 7) Claim(s) \_\_\_\_ is/are objected to.
- 8) Claim(s) \_\_\_\_ are subject to restriction and/or election requirement.

#### Application Papers

- 9) The specification is objected to by the Examiner.
- 10) The drawing(s) filed on \_\_\_\_ is/are: a) accepted or b) objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

#### Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) All    b) Some \* c) None of:
  1. Certified copies of the priority documents have been received.
  2. Certified copies of the priority documents have been received in Application No. \_\_\_\_.
  3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

\* See the attached detailed Office action for a list of the certified copies not received.

#### Attachment(s)

- 1) Notice of References Cited (PTO-892)
- 2) Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)  
Paper No(s)/Mail Date 3-10-04.
- 4) Interview Summary (PTO-413)  
Paper No(s)/Mail Date. \_\_\_\_.
- 5) Notice of Informal Patent Application (PTO-152)
- 6) Other: \_\_\_\_.

## **DETAILED ACTION**

### ***Information Disclosure Statement***

1. The information disclosure statement (IDS) submitted on March 10, 2004 is being considered by the examiner.

### ***Claim Rejections - 35 USC § 102***

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 1-20 are rejected under 35 U.S.C. 102(b) as being anticipated by Itoh (U.S. Pat. No. 5,220,530).

Regarding claim 1, Itoh discloses a semiconductor integrated circuit device comprising: a plurality of memory cells (figure 3, array of memory cells), each having a storage MOSFET holding an information in a gate of the storage MOSFET (figure 2, charge storage layer 35 holding an information in the transistor 33), a write transistor supplying a write information voltage corresponding to the information to the gate of the storage MOSFET (figure 2, write transistor 34 supplying a write information voltage corresponding to information to the gate of storage transistor 33), and a capacitor having a first terminal and a second terminal (figure 2, capacitor having a first terminal and second terminal connecting to word line at node 36 and to storage transistor 33); a plurality of word lines (figure 2, word lines 36, 39; also see figure 3)

coupled with the plurality of the memory cells; and a plurality of data lines (figure 2, write bit line and read bit line; also see figure 3) coupled with the plurality of the memory cells, wherein the first terminal of the capacitor is coupled with one of the plurality of word lines and the second terminal of the capacitor is coupled with the gate of the storage MOSFET (figure 2), wherein, in a read operation of the semiconductor integrated circuit device, the gate voltage of the storage MOSFET is boosted by a transition of the word line from a first voltage to a second voltage greater than the first voltage (in read operation, gate voltage of the storage transistor rise to second level; col. 1, lines 44+; col. 5, lines 18+; col. 7, lines 28+).

Regarding claim 2, Itoh discloses the semiconductor integrated circuit device according to claim 1, wherein the plurality of data lines have a plurality of write data lines and a plurality of read data lines (figure 2, write bit line at node 40 and read bit line at node 37; also see figure 3), wherein each of the plurality of the write data lines is coupled with the write transistor included in each of the plurality of memory cells (figure 2, write bit line 40 is coupled to write transistor 34 of the memory cell), and wherein each of the plurality of the read data lines is coupled with the storage MOSFET in each of the plurality of memory cells (figure 2, read bit line 37 is coupled to storage transistor 33 of the memory cell).

Regarding claim 3, Itoh discloses the semiconductor integrated circuit device according to claim 2, further comprising: a plurality of write control circuits connected between the plurality of read data lines and the plurality of write data lines, respectively, wherein each of the plurality of write control circuits conveys a signal which appeared on a corresponding one of the plurality of read data lines to a corresponding one of the plurality of write data lines (col. 5, lines 51+).

Regarding claim 4, Itoh discloses the semiconductor integrated circuit device according to claim 1, further comprising: a data line select circuit selecting one of the plurality of data lines; and a first and a second common data line coupled with one of the plurality of the data lines selected by the data line select circuit, wherein the first and second common data lines are precharged to a precharge voltage that is between a high level voltage and a low level voltage at a time of amplifying voltages on the first and the second common data lines, and wherein a read information which appears on one of the first and second common data lines is amplified using the precharge voltage of the other of the first and second common data lines as a reference voltage (col. 5, lines 51+).

Regarding claim 5, Itoh discloses the semiconductor integrated circuit device according to claim 4, wherein the same number of data lines are respectively coupled with each of the first and second common data lines via the data line select circuit, and wherein the semiconductor integrated circuit device includes a differential amplifier circuit that amplifies the read information produced on one of the first and second common data lines by a charge share with the read data line selected by the data line select circuit using the precharge voltage of the other of the first and second common data lines as the reference voltage (figures 3 and 7).

Regarding claim 6, Itoh discloses the semiconductor integrated circuit device according to claim 1, wherein the storage MOSFET is set to an OFF state regardless of the write information voltage in a write operation of the semiconductor integrated circuit, wherein, in the read operation of the semiconductor integrated circuit device, the storage MOSFET is set to an ON or OFF state corresponding to the information held in the gate of the storage MOSFET by the transition of the word line from the first voltage to the second voltage (col. 7, lines 28+).

Regarding claim 7, Itoh discloses the semiconductor integrated circuit according to claim 1, wherein each of the plurality of word lines is coupled with the gate of the write transistor and the gate of the storage MOSFET (figure 2).

Regarding claim 8, Itoh discloses the semiconductor integrated circuit device according to claim 1, wherein the write transistor 34 is formed above the storage MOSFET 33 (figure 1).

Claims 9-15 and 16-20 contain the similar limitation as previously discussed in claims 1-8. Therefore, they are analyzed as previously discussed with respect to claims 1-8.

### ***Double Patenting***

4. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and, *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

5. Claims 1-20 are rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claims 1-7, 9-14 and 17-18 of U.S. Patent No. 6,515,892. Although the conflicting claims are not identical, they are not patentably distinct from each other because they are claiming the same scope of the invention.

***Conclusion***

6. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Forbes (U.S. Pat. No. 5,995,410)

7. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Gene N Aduong whose telephone number is (571) 272-1773.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, David Nelms can be reached on (571) 272-1787. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

GA  
June 23, 2004



Gene N Aduong  
Primary Examiner  
Art Unit 2818